Reproducible research on microarchitectural attacks

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February 12, 2020–Xug meeting, Rennes, France

Reproducible research, it's a good idea, right?

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- Compromise: some researchers publish the “basic blocks”
  - hope: it’s sort of working, script kiddies can’t use it, experts can modify it for their own research
  - reality: nobody can use it/it depends on how persistent your PhD student is

  $\rightarrow$ some crucial details are left out and there are magic numbers everywhere

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  - it's getting better, but so far: if the paper says it runs on two different CPUs that are somewhat recent, we're good!
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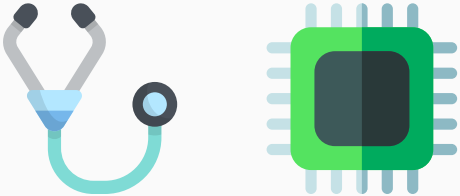
2. I need a pool of heterogeneous machines (mostly different generations)

   $\rightarrow$ I hoard laptops forever so I can keep a Sandy Bridge CPU.

What do I do: Side channels on microarchitecture



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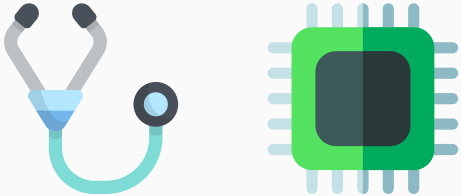

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- For example: the cache leaks information, but how you can exploit it depends on some properties of the cache (inclusivity, level of cache targeted…), and of the environment (native code, JS, ARM vs x86…)

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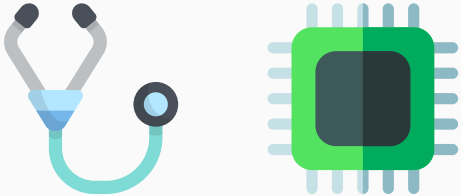

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→ Basically: find a sequence of instructions that does what I want

Why is it so complicated?

Part I: The Good

a.k.a.
Problems I don’t have

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I don’t need:

- fancy clusters
- a lot of memory
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→ I usually just use my own laptop to run experiments

People running their experiments on IGRIDA or Grid'5000 be like

Software portability

- The attacks do rely on specific implementations, so if the implementation changes that might be over, but that's fair
- I don't (normally) use fancy features that may change from one OS version to the other, or write code that relies on libraries that will break if the version is not the same

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→ Software portability is (mostly) fine

→ Starts to be an issue when you want to automate things

Part II: The Bad

a.k.a.
Problems I have I can live with

My constraints: sharing is not caring

- No VM $\rightarrow$ messes with timing
- No sharing the hardware $\rightarrow$ would pollute the cache/other microarchitectural component

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- Side note: I used Grid'5000 for "Reverse Engineering Intel Last-Level Cache Complex Addressing Using Performance Counters" (RAID 2015)

Part III: The Ugly

a.k.a.
The things that have kept me up many a night

The hardware stack

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- If it is the same generation, there might be changes in the number of cores, in the size of the caches, associativity…
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  - → truly engineering: usually okay for your own code, less so if you have code from somebody else with magic values…
- Roughly one new generation per year, and changes can be quite big
  - that part is the biggest issue

Example #1: Last-level cache complex addressing

Example #2: Cache replacement policy

Reproducing results on another machine might be a scientific contribution (and a top tier paper)

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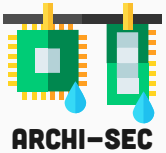
  → virtually nobody cares in the community, but I do care (ANR on this topic)



A new hope?

Artifact Evaluation

- Common in some computer science communities, new in security
- ACSAC (since 2017?), USENIX Security (since 2020), WOOT (since 2019)
- Incentive for reproducible research?
- Artifacts are still not part of the evaluation of the paper